REMARKS

Claims 1-18 are pending; and of these, claims 2 and 11 have been cancelled and claims 1, 5, 6, 8-10, 14, 15, 17 and 18 have been amended. New claim 32 has been added. Accordingly claims 1, 3-10 and 12-18 and 32 are presented for examination.

Claims 19-31 have been cancelled in accordance with the election made without traverse in the reply filed on 03/28/2008.

Claims 1-6, 9-15 and 18 were rejected under 35 USC 102(b) as being anticipated by Ulybin (SU 1619279). Claims 7 and 16 were rejected under 35 USC 103(a) as being unpatentable over Ulybin and further in view of Pierret et al. (US Patent No. 5,079,496). Claims 8 and 17 were rejected under 35 USC 103(a) as being unpatentable over Ulybin and further in view of Aslin et al. (US Patent No. 4,943,919). Applicants have amended independent apparatus claim 1 as well as independent method claim 10, corresponding to independent claim 1, and with respect to these claim, and their respective dependent claims, the Examiner's rejection is respectfully traversed.

Applicants have amended independent apparatus claim 1 to better define Applicants' invention. More particularly, claim 1 has been amended to recite an electronic system comprising both a system to be monitored and a plurality of fault-monitoring systems, the fault-monitoring systems adapted to receive inputs from the system to be monitored and to output a fault signal when any input indicates that the system to be monitored is in a fault condition and the fault-monitoring systems arranged in a cascade fashion such that a fault signal output from one fault-monitoring system is provided as an input to a subsequent fault-monitoring system in the cascade of fault monitoring systems to simulate a fault condition associated with the subsequent fault-monitoring system and the output of a final fault-monitoring system in the

cascade is used as an indicator of a fault in one of the fault-monitoring systems. Applicants' independent method claim 10 has been amended in a manner corresponding to Applicants' independent claim 1, as amended.

The construction recited in Applicants' independent claim 1 is not taught or suggested by Ulybin. More particularly, there is no teaching or suggestion of, as is claimed in Applicants' amended claim 1, of an electronic system comprising a system to be monitored and a plurality of fault-monitoring devices wherein the plurality fault-monitoring devices are adapted to monitor a plurality of input signals from the system to be monitored so as to detect a fault in the system to be monitored. Furthermore, there is no teaching or suggestion, as is also claimed in Applicants' amended claim 1,of the fault-monitoring devices arranged in a cascade fashion and the electronic system adapted to cause the first fault monitoring device of the cascade to detect a fault and to output a fault signal such that a fault signal output from one fault-monitoring device is provided as an input to a subsequent fault-monitoring device in the cascade of fault-monitoring devices to simulate a fault condition associated with the subsequent fault-monitoring device, and the output of a final fault-monitoring device in the cascade is used as an indicator of a fault in one of the fault-monitoring devices.

Specifically, Ulybin discloses a fault simulation device used to purposely insert faults into a calculation process so as to test the fault tolerance of a computing system. See page 2, lines 17-18; page 3, lines 19-21. As shown in Fig. 1, to prepare the fault insertion device for operation, a fault insertion address and a fault signal are stored in a counter with the device. See page 7, lines 17-24. In operation, while the computing system is performing a calculation, the current page address of the computing system and the signal at that address within the computing system are fed as inputs to the fault insertion device. If the current page address is different than

the stored fault insertion address, the signal at the current page address is passed thought the fault insertion device unchanged for use in the calculation being processed on the computing system. However, if the current page address and the stored fault insertion address are the same, the stored fault signal, and not the signal at the current page address, is read out of fault insertion device and passed out for use in the calculation being processed on the computing system. Once the calculation is finished, the resulting product is evaluated by an undisclosed method to determine the fault tolerance of the computing system. Therefore, rather than detecting an unexpected fault occurring in a system's normal course of operation as recited in the present application, Ulybin purposely creates a faulty calculation product by inserting a fault signal at a predefined memory location within a computing system performing the calculation. Accordingly, while Ulybin does disclose a fault insertion device which simulates faults in a calculation process so as to determine the fault tolerance of the computing system processing the calculation, it does not disclose an electronic system comprising a system to be monitored and a plurality of fault-monitoring devices wherein the plurality fault-monitoring devices are adapted to monitor a plurality of input signals from the system to be monitored so as to detect a fault in the system to be monitored.

Ulybin further discloses a cascade of fault insertion devices to ensure an accurate definition of the place for fault insertion in the calculation process. See page 3, line 23-24. As shown in Fig. 2, a first fault insertion device in the cascade provides identification of a current memory page address, a second device provides identification of a specific command address with the identified memory page address and a third device provides identification of a micro code address within the identified command address and provides a fault signal to be inserted into the calculation at that identified address. Therefore, while Ulybin does disclose a cascade of

fault insertion devices which provides an accurate identification of a fault insertion address, it does not disclose a means of cascade of fault insertion devices which provides a means of determining whether there is a fault with any one of the fault insertion devices within the cascade. Accordingly, while Ulybin does disclose a cascade configuration of fault insertion devices which provides added flexibility in defining a fault insertion address, it does not disclose the fault-monitoring devices arranged in a cascade fashion and the electronic system adapted to cause the first fault monitoring device of the cascade to detect a fault and to output a fault signal such that a fault signal output from one fault-monitoring device is provided as an input to a subsequent fault-monitoring device in the cascade of fault-monitoring devices to simulate a fault condition associated with the subsequent fault-monitoring device, and the output of a final fault-monitoring device in the cascade is used as an indicator of a fault in one of the fault-monitoring devices.

Therefore, Applicants' amended claims 1 and 10, and those claims dependent thereon, all of which recite such features, patentably distinguish over Ulybin.

Moreover, the cited Pierret et al. and Aslin et al. references do not disclose or suggest those limitations recite in amended independent claims 1 and 10 and missing from Ulybin. Pierret et al. discloses a regulator for regulating the excitation voltage of an alternator for charging the battery of an automobile. As shown in Fig. 2a, the regular disclosed in Pierret et al. is comprised of a battery voltage sensing circuit 1, an alternator phase voltage amplitude sensing circuit 2, an alternator field coil excitation control and memory means 3, an alternator phase voltage amplitude memory means 4, an alternator rotation timing means 5, a conditional control logic means 6, a rectifier bridge protection circuit 06, a field coil control 05, a pre-excitation circuit 8, an alternator fault indicator means 9, an excitation sensing circuit 10 and a switching

circuit 92. See col.2, line 61 to col. 8 line 53. This regulator configurations provides for, among other benefits, removal of the risk of full-field excitation of the field coil of the alternator and reduction of the regulator's sensitivity to spurious signal on the alternator phase voltage input. Therefore, while Pierret et al. does disclose a regulator specifically designed for use with an alternator, it does not disclose or suggest an electronic system comprising a system to be monitored and a plurality of fault-monitoring devices wherein the plurality fault-monitoring devices are adapted to monitor a plurality of input signals from the system to be monitored so as to detect a fault in the system to be monitored. Furthermore, Pierret et al. does not disclose or suggest fault-monitoring devices arranged in a cascade fashion and the electronic system adapted to cause the first fault monitoring device of the cascade to detect a fault and to output a fault signal such that a fault signal output from one fault-monitoring device is provided as an input to a subsequent fault-monitoring device in the cascade of fault-monitoring devices to simulate a fault condition associated with the subsequent fault-monitoring device, and the output of a final fault-monitoring device in the cascade is used as an indicator of a fault in one of the fault-monitoring devices. Rather, Pierret et al. discloses a single regulator sensing and acting upon a battery voltage input and an alternator phase voltage input.

Aslin et al. discloses an onboard central maintenance computer system comprising, as shown in FIG. 1, multiple line replacement units 14, a communication system 16, a central maintenance computer 12 and an operator interface device 18. The line replacement units 14 continuously communicate fault data directly to the central maintenance computer 12 via the communication system 16 using a standard data transmission protocol. The central maintenance computer 12 communicates data and status information about the line replaceable units 14 to operator interface device 18. The operator interface device 18 may also be used to initiate a test

of line replaceable units 14 through a test initiation bus 48. Therefore, Aslin et al. does not disclose or suggest fault-monitoring devices arranged in a cascade fashion and the electronic system adapted to cause the first fault monitoring device of the cascade to detect a fault and to output a fault signal such that a fault signal output from one fault-monitoring device is provided as an input to a subsequent fault-monitoring device in the cascade of fault-monitoring devices to simulate a fault condition associated with the subsequent fault-monitoring device, and the output of a final fault-monitoring device in the cascade is used as an indicator of a fault in one of the fault-monitoring devices. Rather, Aslin et al. discloses line replacement units communicating fault data directly to the central maintenance computer via the communications network and the central maintenance computer initiating a test of the line replaceable units via the test initiator bus.

Accordingly, Pierret et al. and Aslin et al. fail to add those limitation recited in amended claims 1 and 10 and missing from Ulybin. Therefore, applicants' amended claims 1 and 10, and their respective dependent claims, patentably distinguish over the combination of the Ulybin, Pierret et al. and Aslin et al. references.

As such, it is requested that independent claims 1 and 10, and dependent claims 3-9, 12-18 be allowed.

New claim 32 is presented that recites the limitation of a record of a fault from the output of the final fault-monitoring system, the absence of a record being created signifying a fault in a fault-monitoring device. Support for this feature is shown at least on page 4 line 8 of the specification. The allowance of claim 17 is solicited.

In light of the foregoing, reconsideration and allowance of this application are respectfully requested.

Respectfully submitted,

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